

MODEL: MG4251B03-1

Ver. 1.1

Date: 31.Oct.2019

Customer's A	Approval	СЅОТ	
Signature	Date	Approved By Product Director	Date
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		Reviewed By PM	Date
		Name:	
		Signature:	

Revision History

Version	Date	Page	Section	Description	Revision by
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1. GENERAL DESCRIPTION

1.1 Introduction

MG4251B03-1 is a diagonal 42.5" color active matrix LCD open cell with 2ch-LVDS interface. This open cell is a transmissive type display operating in the normally black mode. It supports 1920*1080 FHD resolution and can display up to 16.7M colors(8bit) Each pixel is divided into Red .Green and Blue sub-pixels which are arranged in vertical stripe.

1.2 Features

- LCM brightness 500 nits
- contrast ratio. 4000:1
- response time 6.5ms.
- High color saturation.
- FHDTV (1920*1080 pixels) resolution.
- DE (Data Enable) only mode.
- LVDS (Low Voltage Differential Signaling) interface.
- RoHS compliance.
- Aspect ratio: 16:9

1.3 General information

Item	Specification	Unit
Bezel Opening Area	961.800(H)*551.250(V)*12.1 (D)	mm
Display area	940.896(H) * 529.254 (V)	mm
Number of Pixel	1920x3(RGB) x1080	pixel
Pixel pitch	0.49005(H) x 0.16335(V)	mm
Pixel arrangement	RGB Vertical Stripe	
Display mode	Transmissive Mode / Normally Black	
Surface treatment	Anti-glare, Haze 2%, Hard Coating (3H)	
Backlight	LED	
Display Orientation	Portrait(turned clockwise based on front view)/Landscape Enabled	

1.4 Mechanical Information

Item	Min.	Тур.	Max.	Unit	
	Horizontal (H)	961.3	961.8	962.3	mm
Module size	Vertical (V)	550.75	551.25	551.75	mm
	Depth (D)	11.9	12.1	12.3	Mm
Weight		-	8.495	-	g

2. ABSOKUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Va	Unit		
nem	Symbol	Min.	Max.	Oilit	
Power Supply Voltage	V_{CC}	-0.3	13.5	V	
Input Signal Voltage	V _{IN}	-0.3	3.6	V	

2.2 Environment Requirement (Based on CSOT's BLU)

(1) Temperature and relative humidity range are shown as below.

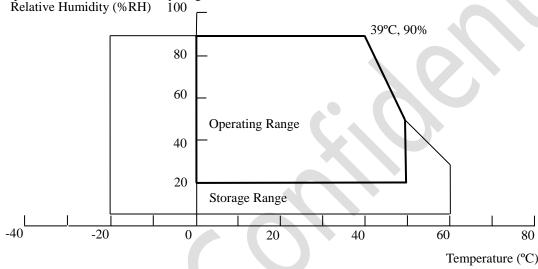


Fig. 2.1 Operating and storage environment

- (a) 90% RH maximum (TA \leq 39 °C).
- (b) Wet-bulb temperature should be 39°C maximum (TA > 39 °C).
- (c) No condensation.
- (2) The storage temperature is between 20 °C to 60 °C, and the operating ambient temperature is between 0 °C to 50 °C. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65°C with LCD module in a temperature controlled chamber alone. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65°C. The range of operating temperature may degrade in case of improper thermal management in the end product design.
- (3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.

2.3 Absolute Ratings of Environment (Open Cell)

When storing open cell as spares for a long time, please follow the precaution instructions:

- (1) Do not store the module in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from 20°C to 30°C in normal humidity ($50 \pm 10\%$ RH) with shipping package.
- (2) The open cell should be keep within one month shelf life.

3. OPTICAL CHARACTERISTICS

3.1 Optical specification

Ite	em	symbol	condition	Min	Тур	Max	Unit	Note	
Contra	st ratio	CR	CR		4000	-		(1)(2)	
Respons	se Time	Gray to gray	у	-	6.5	12	ms	(3)	
Center Lumina	nce of White	LC	0.77	450	500	-	cd/m²		
Cros	stalk	CT-2D	θ X=0	-	-	4	%	(2)(5)	
Luminous	Uniformity		θ y=0	70	75	-	%		
	D - J	RX	Viewing		0.652		-		
	Red	RY	Angle At normal		0.336				
	Croon	GX	Direction		0.317		-		
Color	Color	GY	Direction	Тур	0.618	Тур	-	(2)(6)	
chromaticity	Blue	BX		-0.03	0.153	+0.03	-	(2)(6)	
	Blue	BY			0.050		-		
	W/L:	WX			0.285		-		
	White	WY			0.293		-		
Color	gamut	CG		68	72	-	%		
	III. di maral	θ X+		-	89	-			
Viewing	Horizontal	θ Х-	CD > 10		-	89	-		(7)
angle	West's al	θ y+	CR≥10	-	89	-	doo	(7)	
	Vertical	θ у-		-	89	-	deg		

To measure the module, it is suggested to set up the standard measurement system as Fig. 6.1. The measuring area S should contain at least 500 pixels of the LCD cell as illustrated in Fig.6.2 (A means the area allocated to one pixel). In this model, for example, the minimum measuring distance Z is 370mm when θ is 2 degree. Hence, 500mm is the typical measuring distance. This measuring condition is referred to 301-2H of VESA FPDM 2.0 about viewing distance, angle, and angular field of view definition.

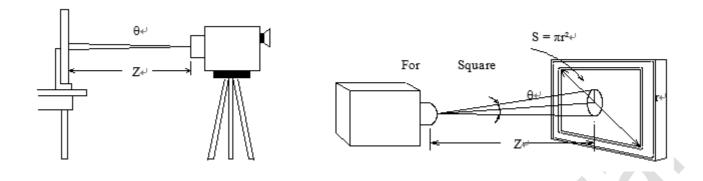


Fig. 3.1 The standard set-up system of measurement measured

Fig. 3.2 The area S contains at least 500 pixels to be

 $N=S/A \ge 500$ pixels

N means the actual number of the pixels in the area S.

Note:

(1) Definition of static contrast ratio (CR):

It's necessary to switch off all the dynamic and dimming function when measuring the static contrast ratio.

CR-W is the luminance measured by LMD (light-measuring device) at the center point of the LCD module with full-screen displaying white. The standard setup of measurement is illustrated in Fig. 6.3; CR-D is the luminance measured by LMD at the center point of the LCD module with full-screen displaying black. The LMD in this item is CS2000.

(2) The LMD in the item could be a spectroradiometer such as (KONICA MINOLTA) CS2000, CS1000 (TOPCON), SR-UL2 or the same level spectroradiometer. Other display color analyzer (KONICA MINOLTA) CA210, CA310 or (TOPCON) BM-7 could be involved after being calibrated with a spectroradiometer on each stage of a product.

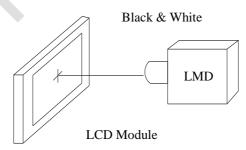


Fig. 3.3 The standard setup of CR measurement

(3) ponse time T_L is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element $t_{X \text{ to } Y}$ is the transition time from luminance ratio X to Y. X and Y are two different luminance ratios among 0%, 25%, 50%, 75%, and 100% luminance. The transition time $t_{X \text{ to } Y}$ is defined as the time taken rom 10% to 90% of the luminance difference between X and Y (X < Y) as illustrated in Fig.6.4. When X > Y, the definition of $t_{X \text{ to } Y}$ is the time taken from 90% to 10% of the luminance difference between X and Y. The response time is optimized on refresh rate $F_r = 60$ Hz.

(4)								
Measured Transition Time		Luminance Ratio of Previous Frame						
		0% 25% 50%		75%	100%			
	0%		t25% to 0%	t _{50% to 0%}	t _{75% to 0%}	t _{100% to 0%}		
Luminance	25%	t _{0% to 25%}		t _{50% to 25%}	t _{75% to 25%}	t _{100% to 25%}		
Ratio of Current Frame	50%	t _{0% to 50%}	t _{25% to 50%}		t _{75% to 50%}	t _{100% to} 50%		
	75%	t _{0% to 75%}	t _{25% to 75%}	t _{50% to 75%}		t _{100% to 75%}		
	100%	t _{0% to 100%}	t _{25% to 100%}	t _{50% to 100%}	t _{75% to 100%}			

 $t_{X \text{ to } Y}$ means the transition time from luminance ratio X to Y.

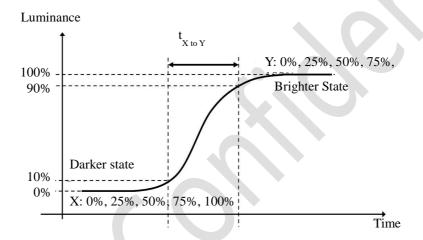


Fig. 3.4 The definition of $t_{X \text{ to } Y}$

All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

4) Definition of center Transmittance (T %):

The transmittance is measured with full white pattern (Gray 255)

(5) Definition of the crosstalk(CT-2D):

YA = Luminance of measured location without gray level 255 pattern (cd/m²)

YB = Luminance of measured location with gray level 255 pattern(cd/m²)

Definition of the crosstalk:
$$CT = YB-YA$$

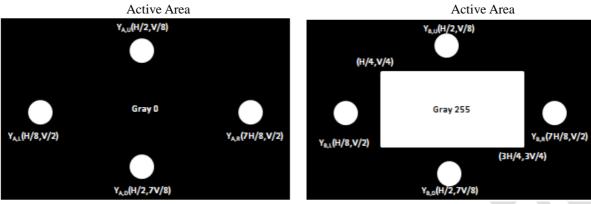


Fig. 3.5 The definition of 2D mode crosstalk

(6) Definition of color chromaticity:

Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying primary color R, G, B and white. The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1953 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 6.6.

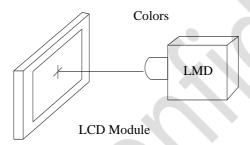


Fig. 3.6 The standard setup of color chromaticity measurement

(7) Definition of viewing angle coordinate system (θ_H , θ_V):

The contrast ratio is measured at the center point of the LCD module. The viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the LCD module (two vertical angles: up θ_{V+} and down θ_{V-} ; and two horizontal angles: right θ_{H+} and left θ_{H-}) as illustrated in Fig. 6.7. The contrast ratio is measured by ELDIM EZ Contrast.

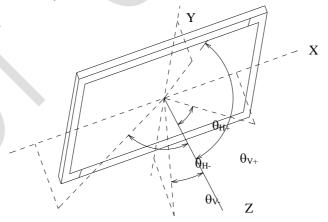


Fig. 3.7 Viewing angle coordination system

4. INTERFACE PIN CONNECTION

4.1 Interface pin assignment

CN1: FF01-41T-5131 (FCN) or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	NC	No Connection	
2	NC	No Connection	
3	NC	No Connection	

NC NC	No Connection	
NC	No Connection	
NG	No Connection	
NC	No Connection	(2)
LVDS_SEL	LVDS Data Format Selection	(2)
	_	
RO[0]P	Odd LVDS Signal +	
RO[1]N	Odd LVDS Signal -	
RO[1]P	Odd LVDS Signal +	
RO[2]N	Odd LVDS Signal -	
RO[2]P	Odd LVDS Signal +	
GND	Ground	
ROCLK-	Odd LVDS Clock -	
ROCLK+	Odd LVDS Clock +	
GND	Ground	
RO[3]N	Odd LVDS Signal -	
RO[3]P	Odd LVDS Signal +	
NC	No Connection	
RE[0]N	Even LVDS Signal -	
RE[0]P	Even LVDS Signal +	
	Even LVDS Signal -	
RE[2]P		
	NC NC NC GND RO[0]N RO[0]P RO[1]N RO[1]P RO[2]N RO[2]P GND ROCLK- ROCLK+ GND RO[3]N RO[3]P NC NC NC NC NC RE[0]N RE[0]P	NC No Connection NC No Connection NC No Connection GND Ground RO[0]N Odd LVDS Signal - RO[0]P Odd LVDS Signal + RO[1]N Odd LVDS Signal - RO[1]P Odd LVDS Signal - RO[2]N Odd LVDS Signal - RO[2]P Odd LVDS Signal - GND Ground ROCLK- Odd LVDS Clock - ROCLK+ Odd LVDS Clock + GND Ground RO[3]N Odd LVDS Signal - RO[3]P Odd LVDS Signal + NC No Connection RE[0]P Even LVDS Signal - RE[1]P Even LVDS Signal - RE[2]P Even LVDS Signal -

44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	NC	No Connection	
48	12V	DC power supply	
49	12V	DC power supply	
50	12V	DC power supply	
51	12V	DC power supply	

Note:

(1) The direction of pin assignment is shown as below:



Fig. 4.1 Connector direction sketch map

Fig. 4.1 LVDS connector direction sketch map

(2) High: connect to $+3.3 \text{ V} \rightarrow \text{VESA}$ format; Low: connect to GND or Open $\rightarrow \text{JEIDA}$ format.

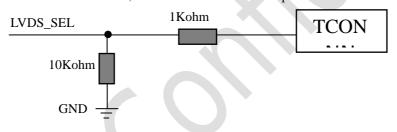


Fig. 4.2 LVDS_SEL PCBA set

4.2 Block Diagram of Interface

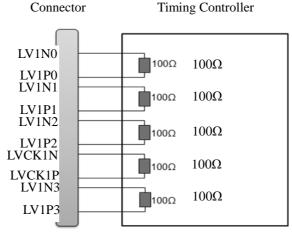


Fig. 4.4 Block diagram of interface

Attention:

- (1) This open cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.
- (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

4.3.1 VESA Format (SELLVDS = H)

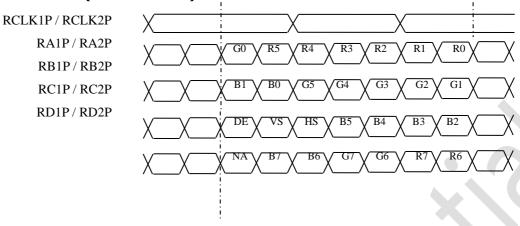
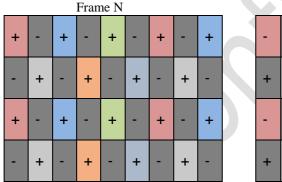
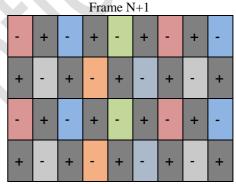


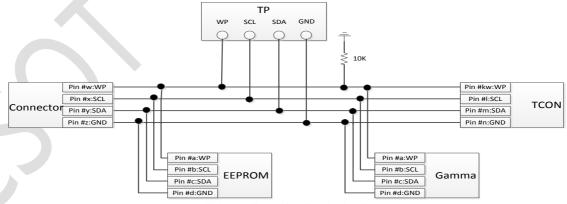
Fig. 4.6 VESA format

4.4 V-com Adjustment

■ Flicker Pattern (L128)







Flicker Adjust Circuit Block Diagram

5. Electrical Specifications

5.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Cromb of		Value	Unit	Note		
		Symbol	Min.	Тур.	Max.	Oint	Note	
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)	
Rush Current		IRUSH	-	-	1.82	A	(2)	
	White Pattern	I_{CC}	-	0.324	0.401	A		
Power Supply Current	Horizontal Stripe	I _{CC}	-	0.707	0.816	A	(3)	
	Black Pattern	I _{CC}	-	0.323	0.399	A		

Note:

- (1) The ripple voltage should be controlled less than 10% of V_{CC} .
- (2) Measurement condition: $V_{CC} = 5V$, Rising time = $470\mu s$.

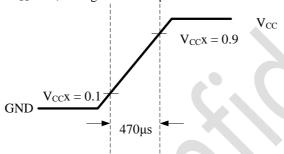
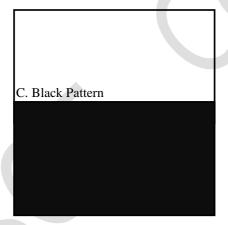


Fig. 3.1 V_{CC} rising time condition

(3) Measurement condition: $V_{CC} = 5V$, $Ta = 25 \pm 2^{\circ}C$, F = 60 Hz. The test patterns are shown as below.

A. White Pattern



B. Horizontal Pattern

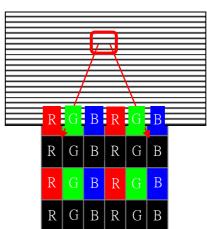


Fig. 3.2 Test patterns

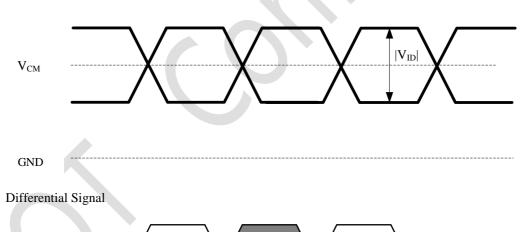
5.2 LVDS Characteristics

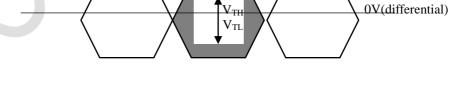
Parameter		Symbol	Value			Unit	Nata
			Min.	Тур.	Max.	Unit	Note
	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	
LVDS Interface	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential Input Voltage	$ V_{ID} $	100	-	600	mV	(1)
	Terminating Resistor	R_{T}	87.5	100	112.5	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
CIVIOS IIITETIACE	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note:

- (1) The product should be always operated within above ranges.
- (2) The LVDS input signal has been defined as follows:

Single end Signals





5.3 Temperature Specifications

Daramatar	Symbol		Spec	I I!4	N	
Parameter		Min.	Тур.	Max.	Unit	Note
Source driver	T _c	-	-	115	$^{\circ}\!\mathbb{C}$	(1)
PMIC	T _C	-	-	100	$^{\circ}$ C	(1)
TCON	T _C	-	-	100	C	(1)

Note:

(1)Any point on the IC surface must be less than Max. specification under any condition, If the surface temperature is out of the specification, thermal solutions should be applied to avoid be damaged;

5.4 Driver IC ESD Specification

The Electro-Static Discharge tolerance of Source COF IC and Gate COF IC is +-2KV tested by ESD Gun. Especially if the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid be damaged, as shown in Fig.3.4 and Fig.3.5.

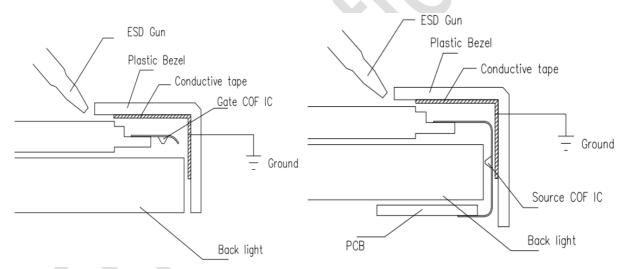


Fig. 3.4 Source COF IC ESD protection

Fig. 3.5 Gate COF IC ESD protection

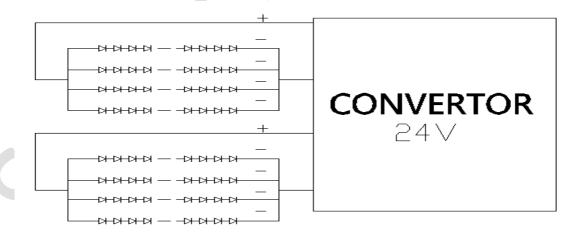
6.Backlight Unit

6.1 LED Converter Input Signal & Power

Parameter	Symbol		Value			Note	
r arameter	Symbol	Min	Тур	Max	Unit	Note	
LED Light Bar Input Voltage	Vo	22	24	26.4	V		
LED Light Bar Input Current 1	Io1	-	2.6		A	Vin=24V,Von/off= 5V,PWM=100%,R L=PANEL	
Power Consumption	Po		64		W	Vin=24V,Von/off= 5V,PWM=100%,R L= PANEL	
Luminous Uniformity		70	75		%		
LED Life Time	LLED	30000			Н	Tj=120℃, L50	

<LED Converter Input Connector Pin Configuration>

Pin No	Symbol	Description
1,2,3,4,5	+24V	Supply voltage(+24V)
6,7,8,9,10	GND	GROUND
11	NC	NO CONNECT
12	ON/OFF	Backlight ON/OFF control
13	Adj	External ADJ control signal
14	NC	NO CONNECT



Lìght Bar Círcuit Dìagram

6.2 Timing Table (DE Only Mode)

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note	
	Frequency	Fclkin (=1/T _{Clk})	65	74.25	80	MHz	(1) (2)	
LVDS	Input cycle to cycle jitter	Trcl			200	ps	(3)	
Receiver Clock	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	1	Fclkin+2%	MHz		
	Spread spectrum modulation frequency	F _{SSM}	0		200	KHz	(4)	
LVDS Receiver Data	Receiver Skew Margin	T_{RSM}	-400	_	400	ps	(5)	
V /	Frame Rate	F	48	60	62.5	Hz		
Vertical Active	Total	T_{V}	1092	1125	1380	T_{H}	$T_V = T_{VD} + T_{VB}$	
Display Term	Display	$T_{ m VD}$		1080				
Term	Blank	T_{VB}	12	45	300	T_{H}		
Horizontal	Total	T_{H}	1046	1100	1174	T_{CLK}	$T_{H} = T_{HD} + T_{HB}$	
Active Display	Display	$T_{ m HD}$		960				
Term	Blank	Тнв	86	140	214	T_{CLK}		

Note:

- (1) The TFT LCD open cell is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.
- (2) Please make sure the range of pixel clock follows the following equations:

 $Felkin(max) \ge Fmax \times Tv \times Th \qquad Fmin \times Tv \times Th \ge Felkin(min)$

Main frequency Max is 96Mhz without spread spectrum

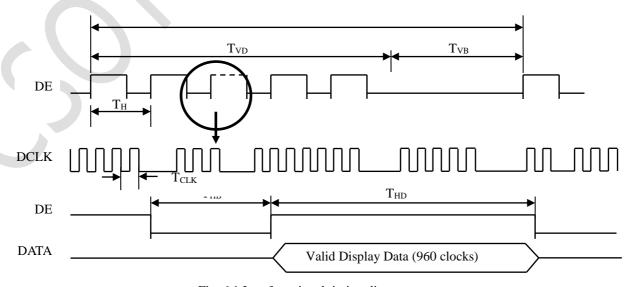


Fig. 6.1 Interface signal timing diagram

(3)The input clock cycle-to-cycle is defined as below figures.

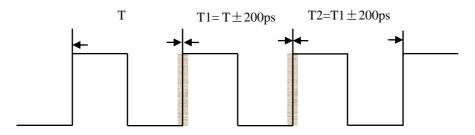


Fig. 6.2 Jitter

(4) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

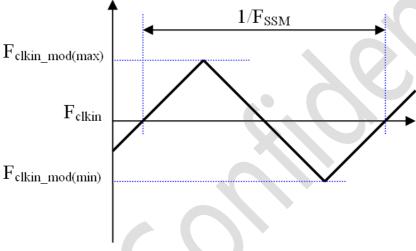


Fig. 6.3 SSCG

(5) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

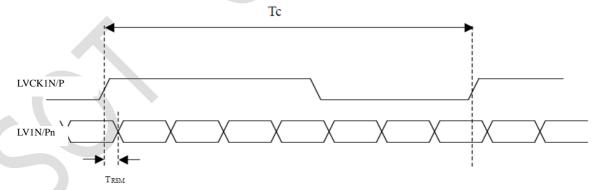


Fig.6.4 LVDS receive interface timing diagram

6.3 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.

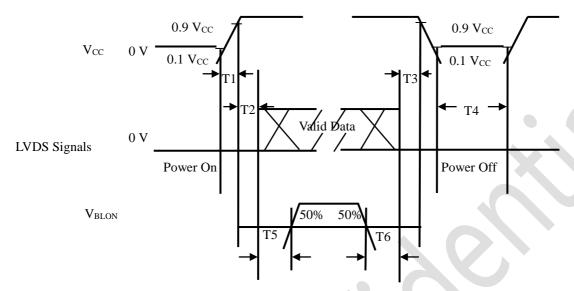


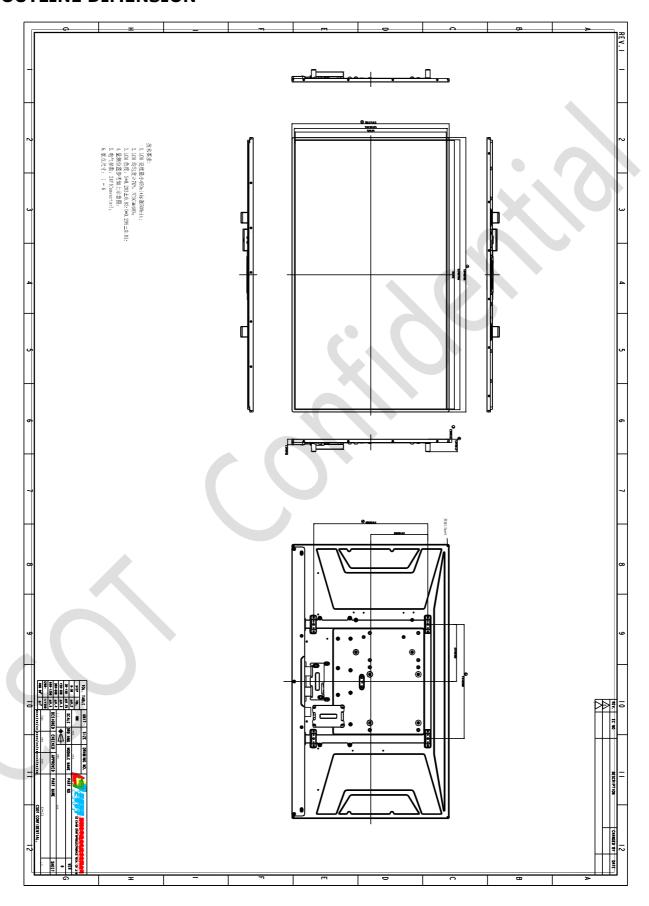
Fig.6.5 Power on/off sequence

D .		Unit		
Parameter	Min.	Typ.	Max.	Min.
T1	0.5		10.0	ms
T2	0.0	-	50	ms
Т3	0.0	<u>J</u> -	50	ms
T4	1000.0	-	-	ms
Т5	500.0	-	-	ms
Т6	100.0	-	-	ms

Attention:

- (1) The supply voltage of the external system for the open cell input should follow the definition of VCC.
- (2) When the customer's backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case that VCC is in off level, please keep the level of input signals on the low or high impedance. If T2 < 0, that may cause electrical overstress.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. OUTLINE DIMENSION

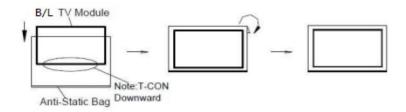


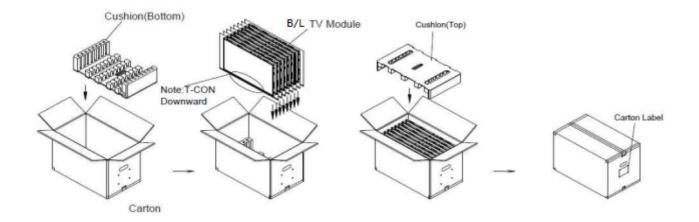
7.2 Packing

7.2.1 Packing Specifications

in the state of th						
Te	Specification					
Item	Quantity	Dimension (mm)	Weight (kg)			
Packing Box	6 pcs / box	660 (L) x 220 (W) x 430 (H)	Net Weight:TBD Gross Weight: TBD			
Pallet	1	1160 (L) x 930 (W) x 120 (H)	Net Weight: TBD			
Stack Layer	1					
Boxes per Pallet	18 box / pallet					
Pallet after Packing	108 pcs / pallet	1160 (L) x 930 (W) x 1410 (H)	Gross Weight:TBD			

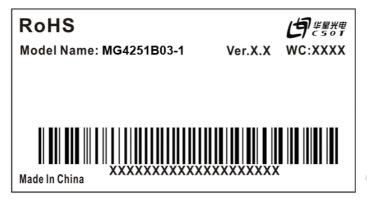
7.2.2 Packing Method

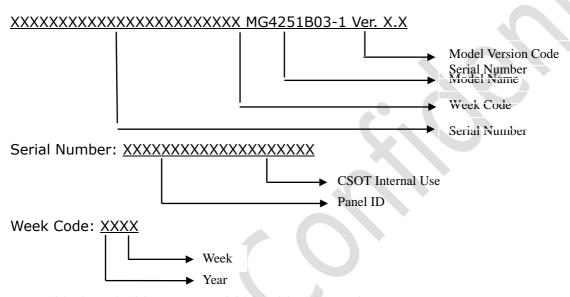




8. Definition of Labels

8.1 Module Label





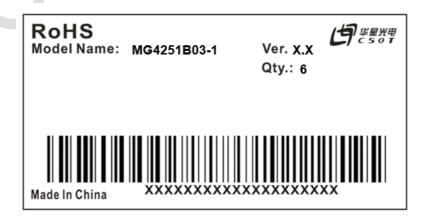
Year: 2010 =10, 2011 = 11 ...2020 = 20, 2021 = 21...

Week: 01, 02, 03 ...

Model Name: MG4251B03-1

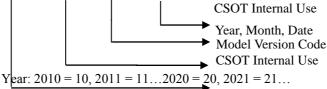
Ver.X.X: Version, for example: 0.1, 0.2, ..., 1.1, 1.2, ..., 2.1, 2.2, ...

8.2 Carton Label



Model Name: MG4251B03-1 Serial Number: XXXXXXXX

Serial Number: XXXXXXXX XX XXXXX XXXXX



Month: 1~9, A~C, for Jan. ~ Dec. Date: 01~31, for 1st to 31st

Model Version Code: Version of product, for example: 01, 02, 11, 12...

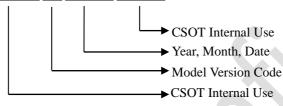
8.3 Pallet Label

Manufactured Date:

内部生成中

Model Name: MG4251B03-1

Serial Number: XXXXXX XX XXXXX XXXXX



10. GENERAL PRECAUTION

10.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

10.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. We do not warrant the module, if customers disassemble or modify the module.

10.3 Breakage of LCD Panel

- 10.3.1. If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.
 - 10.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.
 - 10.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
 - 10.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

10.4 Electric Shock

- 10.4.1. Disconnect power supply before handling LCD module.
- 10.4.2. Do not pull or fold the CCFL cable.

10.4.3. Do not touch the parts inside LCD modules and the fluorescent lamp's connector or cables in order to prevent electric shock.

10.5 Absolute Maximum Ratings and Power Protection Circuit

- 10.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.
 - 10.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
 - 10.5.3. It's recommended to employ protection circuit for power supply.

10.6 Operation

- 10.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.
- 10.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
 - 10.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
- 10.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may cause deformation or color fading.
- 10.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate s olvent.

10.7 Static Electricity

- 10.7.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
- 10.7.2 Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

10.8 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

10.9 Disposal

When disposing LCD module, obey the local environmental regulations.